8/A 01/24/02 D. Bell

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ferguson et al.
Serial No:	09/575,561
Filed:	May 21, 2000
For:	METHOD AND APPARATUS FOR USE IN SWITCHED CAPACITOR SYSTEM
Examiner:	Phan, T.
Art Unit:	2818

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, Washington, D.C. 20231, on November 30th, 2001.

Mark Steinberg

Commissioner for Patents
Washington, D.C. 20231

Sir:

AMENDMENT

In response to the Office Action mailed July 13, 2001 please amend the above-identified application as follows:

01/03/2002 MMOHAMM1 00000003 232825 09575561
02 FC:103 666.00 CH
03 FC:102 168.00 CH
04 FC:104 280.00 CH

In the Specification:

Please amend the specification as follows:

Please amend the paragraph beginning on page 9, line 20 to read as follows:

A1

FIG. 32 shows a three phase clock;

Please amend the paragraph beginning on page 32, line 5 to read as follows:

p2

FIGS. 33A-33C are block diagrams showing the operation of the squaring circuit 500 of FIG. 31 for each of the three clock phases (see FIG. 32) in the event that input terminals 512, 514, 516, 518 are supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 0, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. Referring now to FIG. 33A, on phase P3 of